UNISEC Europe

Objectives

- joint proposals for space outreach activities to be funded by European Union, ESA
- contributions to CanSat educational programs
- joint CubeSat conferences and exchange of experiences
- organization of small satellite ground station networks to support the CubeSat community
- standardization of electrical and software interfaces

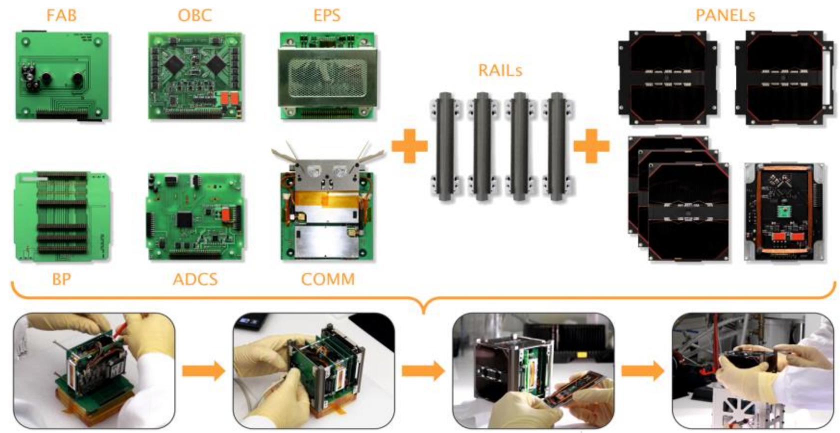
Members

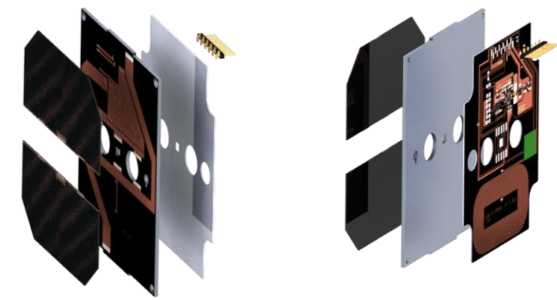
- UNISEC Germany
- UNISEC Lithuania
- UNISEC Samara
- UNISEC Turkey
- ? UNISEC Italy ?
- …

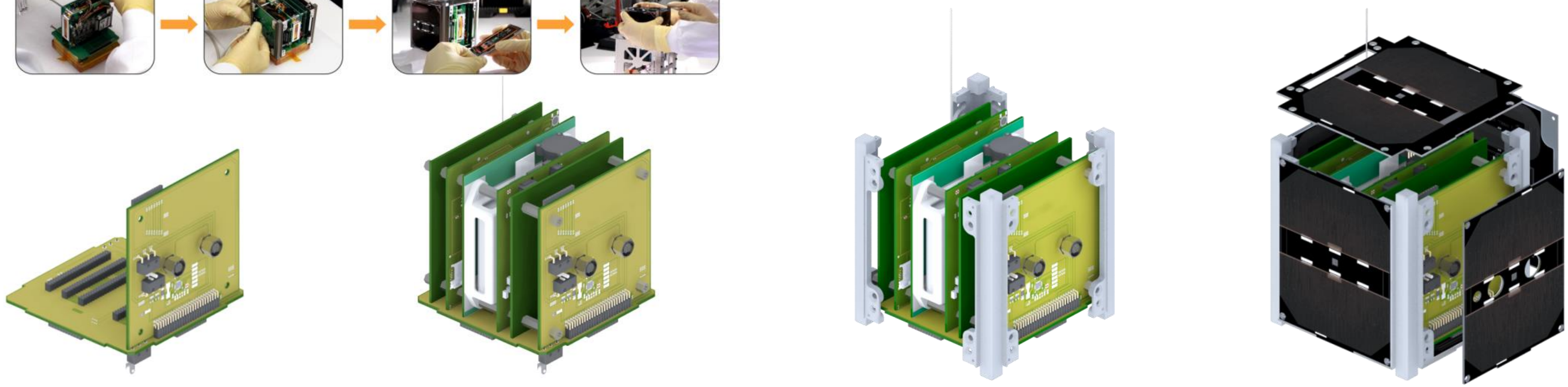
UNISEC EUROPE
University Space Engineering Consortium

http://unisec-europe.eu/

Standardization of Electrical Interfaces / Modular Bus







Advantages:

- Success of CubeSat based on standard regarding dimensions
- Exchange of components at subsystem level
- Much easier way for cooperations

Standardization of Electrical Interfaces

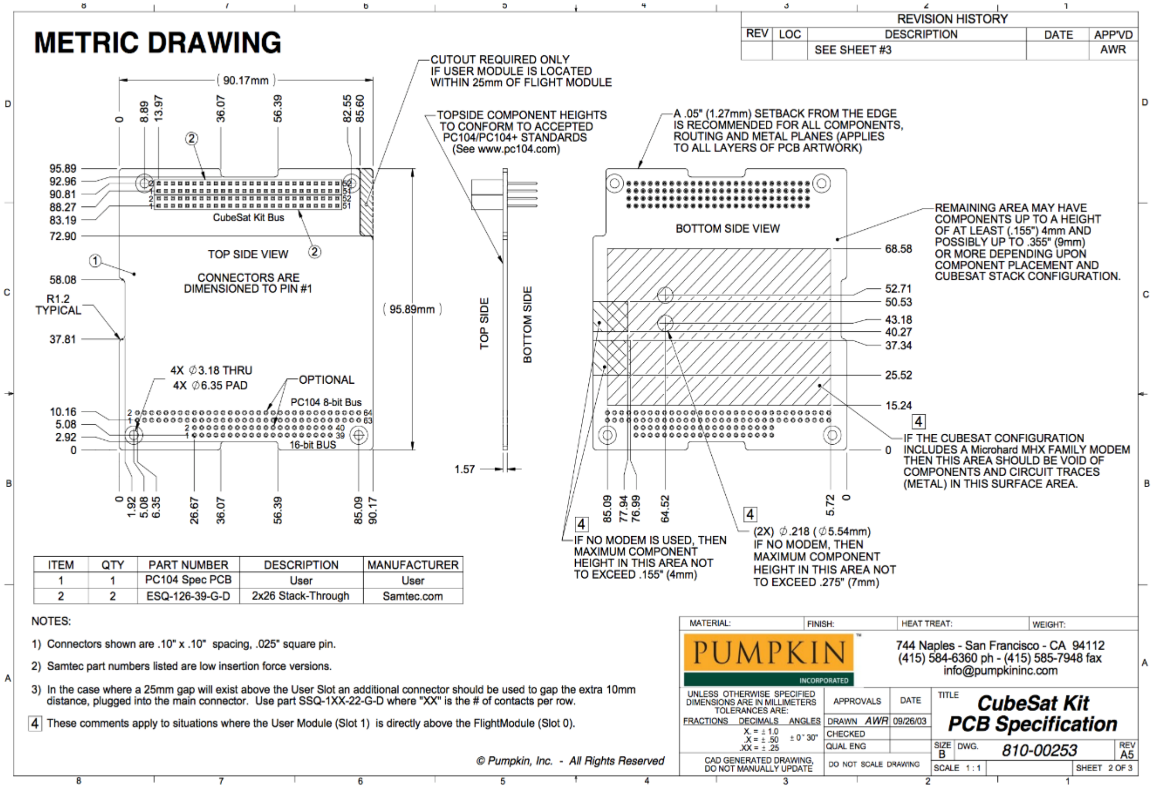
CubeSat Subsystem Standardization

[Image from: CubeSat Kit FM430 Flight Module Hardware Revision: C Manual]

- PC/104 CubeSat Kit Bus
  - often adopted by commercial suppliers (30%)
- Which aspects would we like to carry over to a commonly defined standard due to their technical advantages for pico- and nano-satellites?
(ignoring the fact that many suppliers adopt PC/104 CubeSat Kit Bus)
- Which aspects should be improved?
- Which relevant aspects are not addressed by PC/104?

Existing Mechanical Interface: PC104

- PC/104 CubeSat Kit Connector
  - relatively large in PCB footprint (10%-15%) and height (15mm or 25mm, significant impact for 1U)
  - only a fraction of the 104 Pins usually used
- Board Layout
  - mounting hole alignment could be symmetric
  - metric units?



CubeSat Kit [Product Flyer] http://www.cubesatkit.com/docs/cubesatkitflyer.pdf

Mechanical Interfaces

- Stacking Principle
  - all signals pass all connectors between source and sink:
    - increased power loss (low voltages/ high currents) and noise
- Backplane, Flex-Rigid Bus
  - flexible inter-subsystem spacing, flexibility for assembly and disassembly

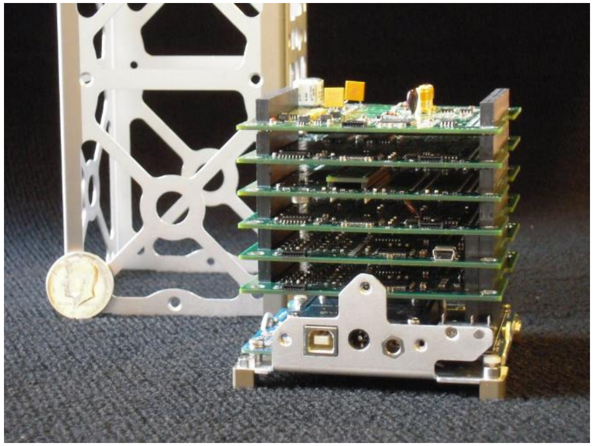
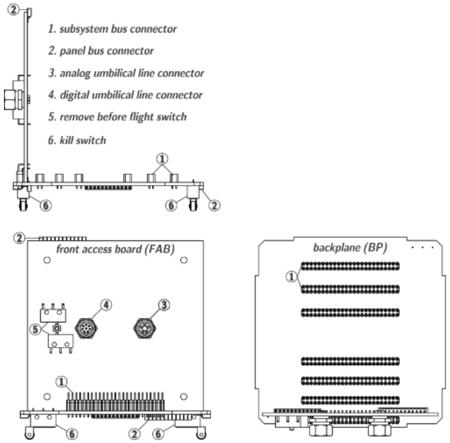
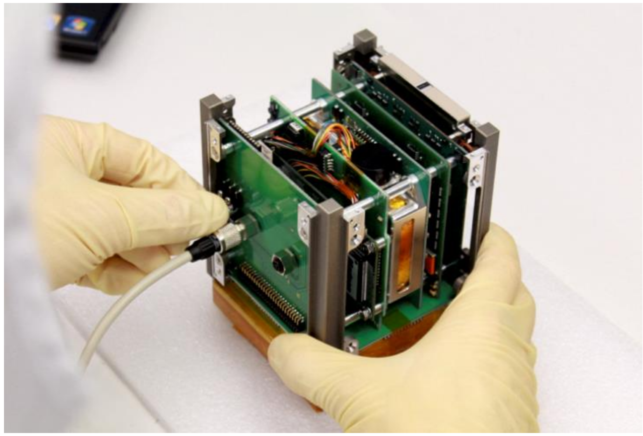
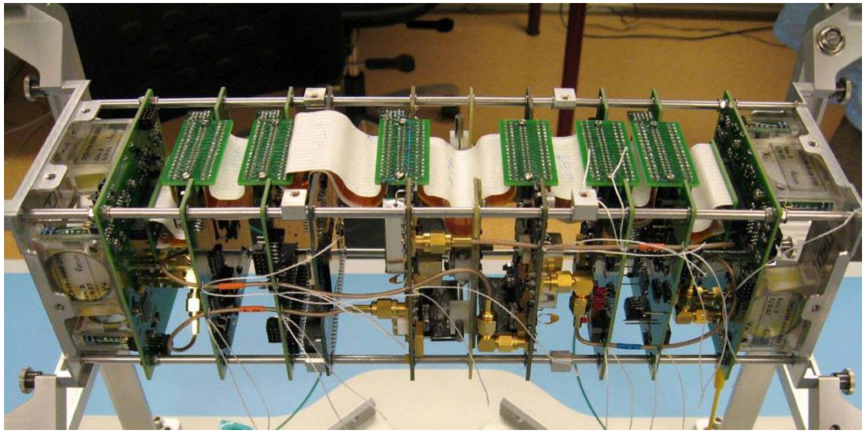


Image from http://www.isde.vanderbilt.edu/wp/wp-content/uploads/vanderbilt_payload.jpg





UWE Bus - University of Wuerzburg



Assembly, Integration and Testing of the Delfi-C3 Nanosatellite
Brouwer, G. F. and Ubbels, W. J. and Vaartjes, A. A. and Hennepe, F. Te
Proceedings of the 59th IAC, Glasgow

Electrical Interface - PC/104 Compliance ff

- only a few lines actually used in common: i.e. comparing pin assignment of:
  - CubeSat Kit Motherboard Rev.E
  - CubeSat Kit Linear EPS Rev.D
  - NanoMind A712C
  - NanoPower P31u-9.0
  - Clyde CubeSat Power Distribution
  - Clyde 3G EPS

		Cubesat Kit		GOM		Clyde	
		CubeSat Kit Motherboard Rev.E	CubeSat Kit Linear EPS Rev.D	NanoMind A712C	NanoPower P31u-9.0	Clyde CubeSat Power Distribution	Clyde 3G EPS
H1	1	GPIO		CANL		SW19	
	2	GPIO				SW19	
	3	GPIO		CANH		SW19	
	4	GPIO	CLK out			SW22	
	5	GPIO				SW23	
	6	GPIO				SW24	
	7	GPIO				A25	
	8	GPIO				A26	
	9	GPIO				A27	
	10	GPIO				A28	
	11	GPIO	ON_SD			A29	
	12	GPIO	GPIO			A30	
	13	GPIO					
	14	GPIO				A31	
	15	GPIO					
	16	GPIO				A32	
	17	RX1	RX1			A9	
	18	TX1	TX1			A33	
	19	RX0	RX0			A10	
	20	TX0	TX0			A34	
	21	SPI CLK	SPI CLK			A11	
	22	SPI MISO	SPI MISO			A35	
	23	SPI MOSI	SPI MOSI			A12	
	24	CS SDcard	CS SDcard			A36	
	25	OC FAULT	OC FAULT			A13	
	26	VREF0				A37	
	27	SENSE				A14	
	28	VREF2				A39	
	29	RESET	RESET			A15	
	30	VREF1				A40	
	31	OFF_VCC				A16	
	32	5V USB	5V USB		5V_in	A32	5V USB
	33	PWR MHX				A17	
	34	RST_MHX				RX	
	35	CTS_MHX				A18	
	36	RTS_MHX				TX	
	37	DSR_MHX				A19	SDA
	38	DXX_MHX				RX1	SCL
	39	TXD_MHX				A20	
	40	RXD_MHX				TX1	
	41	SDA	SDA	SDA	SDA	SDA	SDA
	42	VBACKUP 3V				RX2	GND
	43	SCL	SCL	SCL	SCL	SCL	SCL
	44	RSVDO reserved				TX2	
	45	RSVDO reserved				A21	
	46	RSVDO reserved				RX3	
	47			V PWM	PWR OUT1	A22	
	48			3.3V	PWR OUT2	TX3	
	49			V PWM	PWR OUT3	A23	
	50			3.3V	PWR OUT4	RX4	
	51			V PWM	PWR OUT5	A24	
	52			3.3V	PWR OUT6	TX4	

		Cubesat Kit		GOM		Clyde	
		CubeSat Kit Motherboard Rev.E	CubeSat Kit Linear EPS Rev.D	NanoMind A712C	NanoPower P31u-9.0	Clyde CubeSat Power Distribution	Clyde 3G EPS
H2	1	GPIO Ain				SW1	
	2	GPIO Ain				SW2	
	3	GPIO Ain				SW3	
	4	GPIO Ain				SW4	
	5	GPIO Ain				SW5	
	6	GPIO Ain				SW6	
	7	GPIO Ain				SW7	
	8	GPIO Ain				SW7	Switch1 12V or
	9	GPIO	ON USB			SW7	GND
	10	GPIO				SW8	Switch2 12V or
	11	GPIO				SW9	Switch3 12V or
	12	GPIO				SW10	Switch4 12V or
	13	GPIO				SW11	Switch5 5V
	14	GPIO				SW12	GND
	15	GPIO				SW13	Switch6 5V
	16	GPIO				SW14	Switch7 5V
	17	GPIO				SW14	GND
	18	GPIO				SW14	Switch8 3.3V
	19	GPIO				SW15	Switch9 3.3V
	20	GPIO				SW16	Switch10 3.3V
	21	GPIO				SW17	GND
	22	GPIO				SW18	GND
	23	GPIO				SW2ß	12V
	24	GPIO				SW21	12V
	25	5V	5V		5V	5V	5V
	26	5V	5V		5V	5V	5V
	27	VCC SYS	3.3V	3.3V	3.3V	3.3V	3.3V
	28	VCC SYS	3.3V	3.3V	3.3V	3.3V	3.3V
	29	DGND	GND	GND	GND	GND	GND
	30	DGND	GND	GND	GND	GND	GND
	31	AGND	AGND		AGND	AGND	AGND
	32	DGND	GND		GND	GND	GND
	33	S0	S0				
	34	S0	S0				
	35	S1	S1				PCM in
	36	S1	S1				PCM in
	37	S2					RBF SW
	38	S2					RBF SW
	39	S3					SEP SW1
	40	S3					SEP SW2
	41	S4	S4				BCR OUT
	42	S4	S4				BCR OUT
	43	S5	S5				BCR OUT
	44	S5	S5				BCR OUT
	45	VBATT 7-10V	VBATT 7-10V		V_BAT	Battery	BAT
	46	VBATT 7-10V	VBATT 7-10V		V_BAT	Battery	BAT
	47					RS422 RX A	GND
	48					RS422 TX A	GND
	49					RS422 RX B	
	50					RS422 TX B	
	51					optional V	
	52					optional V	

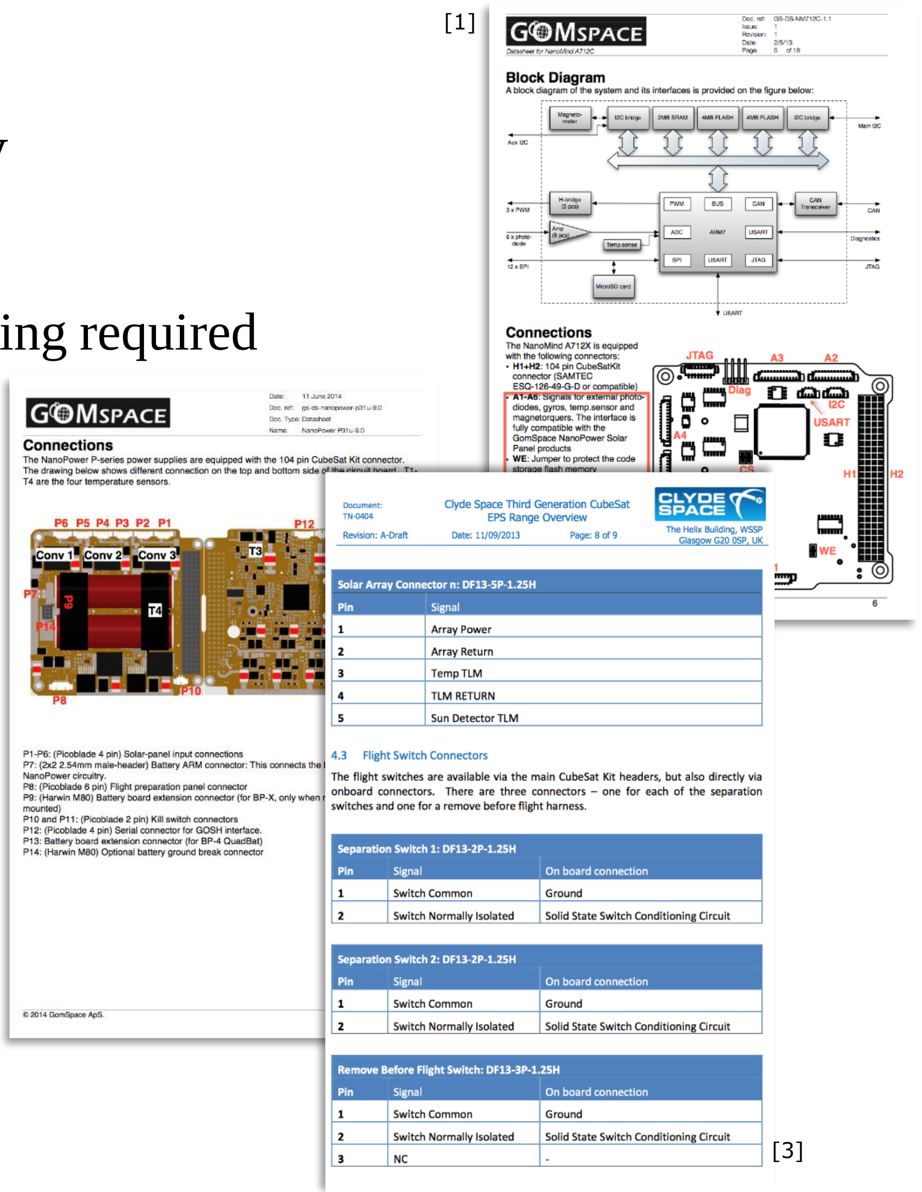
- common signals:
  - 5V charge_in (1 pin)
  - I2C SDA (1 pin)
  - I2C SCL (1 pin)
  - 5.0V (2 pins)
  - 3.3V (2 pins)
  - GND (3 pins)
  - AGND (1 pin)
  - V Battery (2 pins)

Electrical Interface

- many important signals are currently not present on main connector
  - often extra connectors used / wired harnessing required
    - solar panel inputs
    - flight/kill switch logic
    - test, debug, programming interface for individual subsystems
- often missing signals
  - e.g. sync signal for time/clock synchronization between subsystems

[1]

[2]

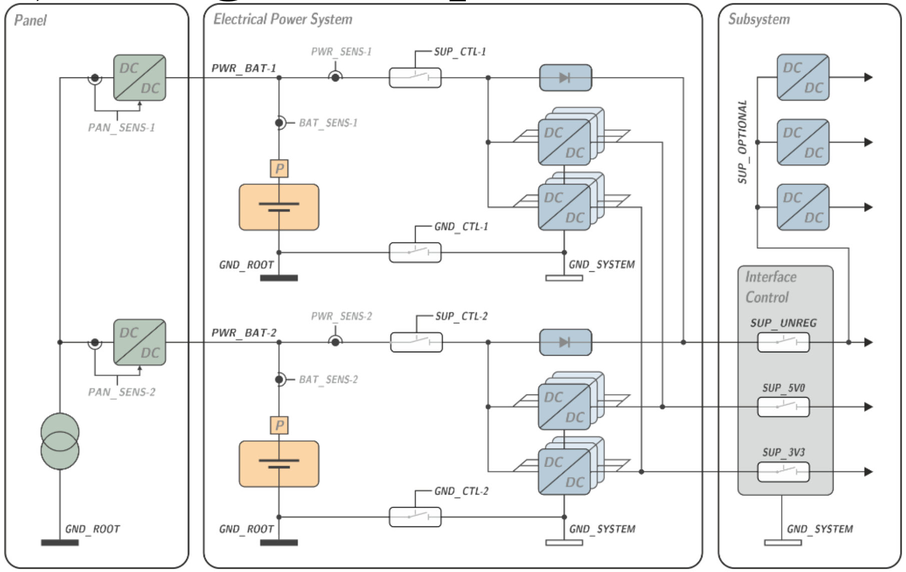


[3]

[1] NanoMind A712C [Product Datasheet]
http://gomspace.com/documents/GS-DS-NM712C-1.1.pdf
[2] NanoPower P-series [Product Datasheet]
http://gomspace.com/documents/gs-ds-nanopower-p31u-9.0.pdf
[3] Clyde Space Third Generation CubeSat EPS Range Overview
http://www.clyde-space.com/documents/3016

Common Standard Recommendations

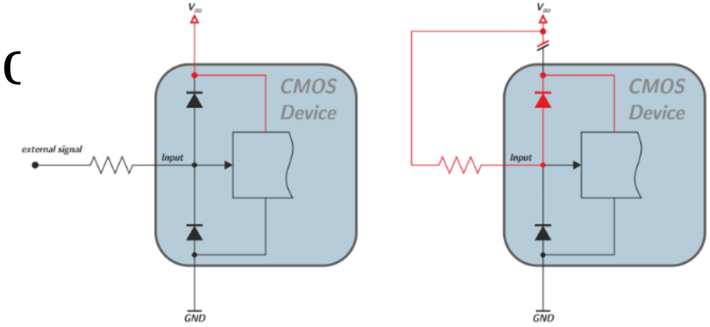
- support for distributed power generation
  - MPPT circuitry can be part of "more intelligent" solar panels
  - can directly supply (redundant) unregulated power bus
    - Minimal impact on required signals on satellite bus
    - Power System capabilities scale with connected power generators
    - Optimal design of MPPT circuitry w.r.t. solar panel
    - Supports arbitrary number of panels with heterogeneous performance



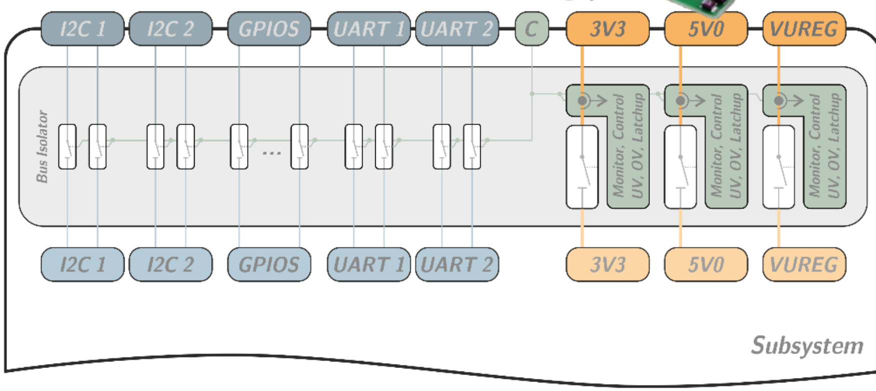
University of Wuerzburg UWE-3 Electrical Power System

Common Standard Recommendations

- specify standardized subsystem interface cc implementing:
  - power switch, monitoring, protection (OV, UV, OC)
    - Optimized for actual subsystem
    - Minimizes impact on required signals on satellite bus (no dedicated switched power line for each potential subsystem)
  - selective isolation of data interface from satellite bus
    - Required for proper partial power down, avoids current leakage for switched off subsystems
    - Can also handle data bus or power bus redundancy selection in a standardized way



undesired current leakage via data interface of powered down CMOS device

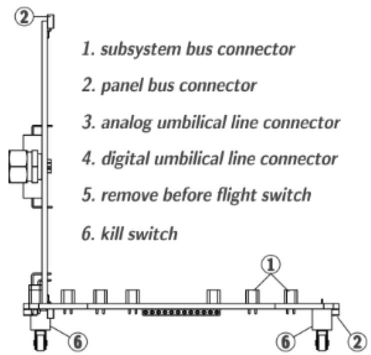


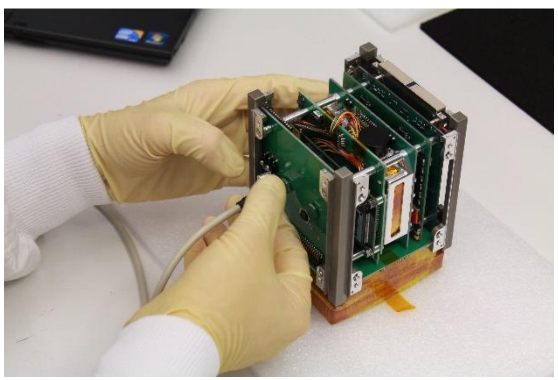
University of Wuerzburg UWE-3 Standard Interface Control Circuit

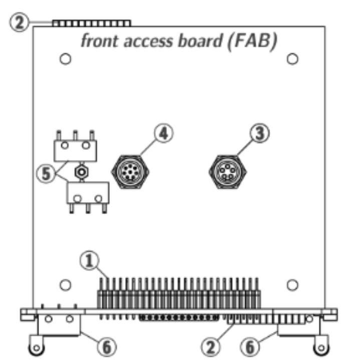
Example UNISEC Europe Bus

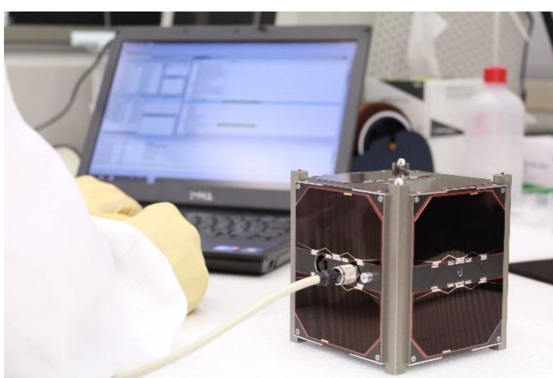
UNISEC EUROPE
University Space Engineering Consortium

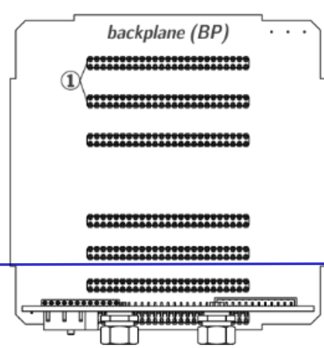
http://unisec-europe.eu/standards/bus/





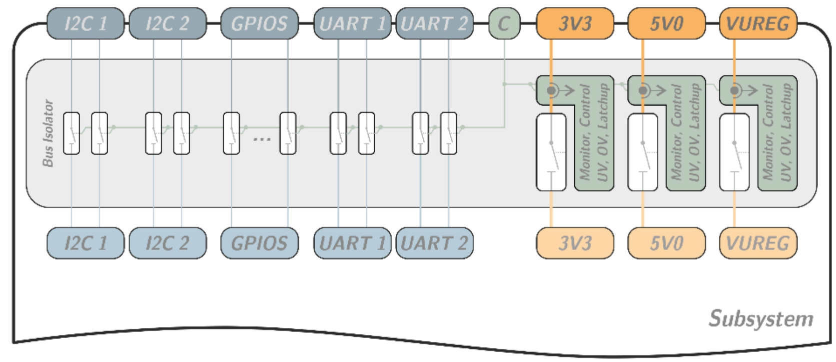


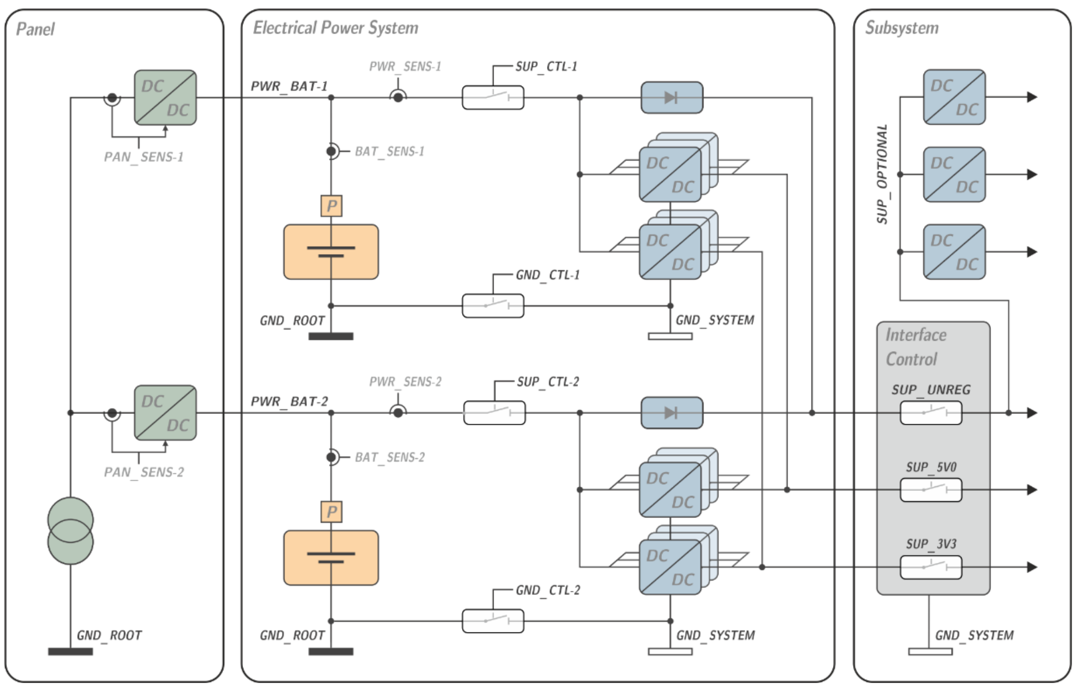




UML_UART (RXD)	1	2	UML_UART (TXD)
UML_SBW-1 (TDIO)	3	4	UML_SBW-1 (TCK)
UML_SBW-2 (TDIO)	5	6	UML_SBW-2 (TCK)
BUS_I2C-1 (SDA)	7	8	BUS_I2C-1 (SCL)
BUS_JTAG (TDI)	9	10	BUS_JTAG (TCK)
BUS_JTAG (TDO)	11	12	BUS_JTAG (TMS)
GND_SYSTEM	13	14	GND_SYSTEM
SUP_5V0	15	16	SUP_5V0
CTL_RESET	17	18	CTL_RESET
COM_UART-1 (RXD)	19	20	BUS_I2C-2 (SDA)
COM_UART-1 (TXD)	21	22	BUS_I2C-2 (SCL)
SUP_UNREG	23	24	SUP_UNREG
SUP_3V3	25	26	SUP_3V3
PWR_BAT-2	27	28	PWR_BAT-2
PWR_BAT-1	29	30	PWR_BAT-1
reserved (PWR_SC_Y)	31	32	reserved (PWR_SC_X)
reserved (PWR_SC_Z)	33	34	CTL_SYNC
GND_ROOT	35	36	GND_ROOT
GND_CTL-1	37	38	GND_CTL-2
SUP_BACKUP	39	40	SUP_BACKUP
SUP_CTL-1	41	42	SUP_CTL-2
General Purpose Input/Output	43	44	COM_IRQ
General Purpose Input/Output	45	46	General Purpose Input/Output
COM_UART-2 (TXD)	47	48	General Purpose Input/Output
COM_UART-2 (RXD)	49	50	General Purpose Input/Output

Power Distribution System





Standardization of Electrical Interfaces

3.1.1 SUBSYSTEM INTERFACE DESCRIPTION

The subsystem interface foresees double row high precision PCB connectors in the standard grid pattern 2.00mm (THT).

Backplane Connector: *BLY 2-50, female, Fischer Elektronik*
Subsystem Module: *SLY 4 035-50-Z, male, Fischer Elektronik*

UML_UART (RXD)	1	2	UML_UART (TXD)
UML_SBW-1 (TDIO)	3	4	UML_SBW-1 (TCK)
UML_SBW-2 (TDIO)	5	6	UML_SBW-2 (TCK)
BUS_I2C-1 (SDA)	7	8	BUS_I2C-1 (SCL)
BUS_JTAG (TDI)	9	10	BUS_JTAG (TCK)
BUS_JTAG (TDO)	11	12	BUS_JTAG (TMS)
GND_SYSTEM	13	14	GND_SYSTEM
SUP_5V0	15	16	SUP_5V0
CTL_RESET	17	18	CTL_RESET
COM_UART-1 (RXD)	19	20	BUS_I2C-2 (SDA)
COM_UART-1 (TXD)	21	22	BUS_I2C-2 (SCL)
SUP_UNREG	23	24	SUP_UNREG
SUP_3V3	25	26	SUP_3V3
PWR_BAT-2	27	28	PWR_BAT-2
PWR_BAT-1	29	30	PWR_BAT-1
reserved (PWR_SC_Y)	31	32	reserved (PWR_SC_X)
reserved (PWR_SC_Z)	33	34	CTL_SYNC
GND_ROOT	35	36	GND_ROOT
GND_CTL-1	37	38	GND_CTL-2
SUP_BACKUP	39	40	SUP_BACKUP
SUP_CTL-1	41	42	SUP_CTL-2
General Purpose Input/Output	43	44	COM_IRQ
General Purpose Input/Output	45	46	General Purpose Input/Output
COM_UART-2 (TXD)	47	48	General Purpose Input/Output
COM_UART-2 (RXD)	49	50	General Purpose Input/Output

3.2 PANEL INTERFACE DESCRIPTION

The panel bus is in principle a subset of the subsystem bus. The panel interface foresees single row high precision PCB connectors in the standard grid pattern 2.00mm (SMT).

Backplane Connector: *BLY 6 SMD/ 12, Fischer Elektronik*
Panel Connector: *SLY 7 SMD/ 045/ 12 G, Fischer Elektronik*

GND_SYSTEM	1
SUP_5V0	2
CTL_RESET	3
BUS_I2C-2 (SDA)	4
BUS_I2C-2 (SCL)	5
SUP_UNREG	6
SUP_3V3	7
PWR_BAT-2	8
PWR_BAT-1	9
reserved (PWR_SC)	10
CTL_SYNC	11
GND_ROOT	12

3.3 UMBILICAL LINE

GND_SYSTEM	1
GND_CTL-1	2
GND_ROOT	3
PWR_BAT-1	4
PWR_BAT-2	5

Analog Umbilical Line

GND_SYSTEM	1
UML_UART (RXD)	2
UML_UART (TXD)	3
UML_SBW-1 (TDIO)	4
UML_SBW-1 (TCK)	5
UML_SBW-2 (TDIO)	6
UML_SBW-2 (TCK)	7

Digital Umbilical Line

Offers for cooperations

- International missions emphasizing distributed networked small satellites for applications in Earth observation and telecommunications
- Support in small satellite design
- International cooperation for networked ground stations
- Intensive classes on small spacecraft design (Tunesia, Russia USA, Turkey, Brasil, China, …)
- Participation of students in the „SpaceMaster" program (http://www.spacemaster.uni-wuerzburg.de/)
- Information exchange at Pico- and Nano-Satellite conference (alternating in Berlin and in Würzburg, already 8 conferences, > 100 participants)

Contact: Prof. Dr. Schilling schi@informatik.uni-wuerzburg.de

UNIVERSITÄT WÜRZBURG

8th Pico and Nano Satellite Workshop

Technology for Small Satellite Research

September 15-16, 2015
Würzburg, Germany

www7.informatik.uni-wuerzburg.de/pina2015

Topics

- In orbit experiences
- Small satellite missions
- Distributed small satellite systems
- Subsystem technologies for small satellites
- Payloads for small satellites
- Applications
- Flight opportunities and launchers for Pico satellites
- Educational aspects

Call for Papers and Detailed Information

The call for papers and other information will be provided on the following website:

www7.informatik.uni-wuerzburg.de/pina2015

Würzburg

The city is located near the center of Germany, offers a wide range of recreation and leisure activities together with theaters, open-air concerts, and wine festivals. Located at the shores of the river Main, vineyards, castles, medieval cities and baroque residence palace are characteristic for the region. Würzburg offers a broad range of accommodations facilities at all costs.

Registration

Participants are requested confirm their participation through e-mail latest by August 12th, 2015.

- Registration fee: 70 €

The registration fee covers lunch and coffee breaks expenses for the duration of workshop.

Schedule

- Submission of abstract: July 20, 2015
- Notification of acceptance: August 05, 2015
- Registration closure: August 12, 2015
- Workshop: September 15-16, 2015

Language

The main language of the workshop is English but contributions in both English and German languages are accepted.

Workshop Location

The IFAC symposium will be held at the Informatics building, Turing-Hörsaal, located at Hubland campus of University of Würzburg and can be quickly be reached by public transport from the city center.

Approach

Würzburg can be easily approached by frequent trains directly from Frankfurt airport in about one hour. Two ICE high speed train routes cross pass through Würzburg, as well as three important German motorways, the A3, A7 and A81. Thus access by train or car is very efficient and easy.